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LITERATURE REVIEW ON REVERSIBLE LOGIC GATES AND IRREVERSIBLE LOGIC GATES

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Abstract. In many of the digital system applications the Arithmetic unit used for various applications like addition, subtraction, multiplication and division. All these operations performed by single unit that is called adder. The main goal of the digital system applications is to design the different types of digital system units with power, area and speed are the main constraints. The adders can be designed by using two methods. They are Irreversible logic gates and reversible logic gates. There are several designing methods available in the literature to implement the both reversible and irreversible logic gates. This paper mainly focuses on the design of both reversible and irreversible logic gate techniques. The literature review helps the researchers to know about the various methods and future work on the Digital systems to improve the efficiency of the digital systems.

Keywords: Adder, Reversible logic gates, Digital Systems

1 Introduction

In present days the development of digital system are developed in more efficiently and most flexible way. while designing the digital systems parameter like area, power, speed are plays a key role .most of digital system are deepened on one of the main digital unit, that is adder. So adder plays an important role while designing the digital system. The adder performs the various arithmetic operations like addition, subtraction, multiplication, division. And all these operations are perform only by using the addition operation. The addition operation done by adding two numbers, subtracting operation performed by negating one operand form the complement's method and then adds both negating operand and another operand. The multiplication operation performed by repeated addition operation and the division operation also performed by repeated subtraction. The adders are mainly designed the using the two technologies. There is IRreversible Logic Technology (IRLT), Reversible Logic Technology (RLT). IRLT uses the logic gates which having M number of inputs N, number of outputs .for an example AND, OR etc. RTL having logic gates with same number of inputs and outputs.

The rest of this paper it organized as follows. In section
2 Irreversible Logic Technology (IRLT).
3 Reversible Logic Technology (RLT).
4 Conclusion of the paper.

2 IRREVERSABLE LOGIC TECHNOLOGY (IRLT)

A Basic single full adder unit has two outputs, one carry and one sum for the single two bit addition operation. The n bit addition required the n number of full adders are used to carry of 1st stage full adder unit is given to the 2nd stage full adder and 2nd stage carry out given to 3rd stage full adder . Similarly up to last stage. In this process the next stage unit waits for the previous stage carry output. So, this waiting property simple describes the delay and in this process the carry is ripple to next stage. This adder is called ripple carry adder.

In S. Usha and Ravi .T [1] disused the disadvantages of the RCA and presented a new design to overcome the disadvantages of RCA by providing the hybrid 9T full adder methods. According to the design, the Gate Diffusion Input (GDI) technology is used. This GDI technology uses GDI cell which resembles the CMOS INVERTER and in this GDI cell has three inputs. They are gate, P and N. The gate is connected as input to the both PMOS and NMOS and P is the input to source /drain of PMOS and similarly N is the input to source /drain of NMOS. The standard p-well CMOS and twin well tube process are used to implement the all possible functions. This GDI -9T full adder having the various advantages are compare to previous conventional ripple carry adder, they are number of transistors is reduced and power consumption is minimized, the layout design of this RCA is designed MICROWIND environment with 0.12 micrometer technology but in this 9T hybrid full adder voltage swing problem occurs. To overcome it and it take to Restoration circuit is added in design. So, due to addition of this restoration circuit the size increases.

S.Ravi Kumar, A. Javali, Ramanath J Nayak et al [2] proposed high speed save adder using carry look Ahead adder to come the disadvantage of CSA using RCA. In the design of RCA with provides sum and carry with more time. To over this time consumption the CSA with CLA is used. The CLA is added in the final stage of CSA. This CLA uses mainly two techniques. They are carry generation and carry propagation. The carry generation technique is based on the AND operation and carry propagation is based X-OR operation. This CLA unit no needs to wait for the previous carry to perform operation. This proposed CSA using CLA having advantages like time consumption is reduced and performance of architecture is improved. The CLA using Verilog HDL CSA simulated on both Xilinx ISE simulator on Virtex4 Target Board and cadence and Cadence Encounter 180nm technology for synthesis results. This proposed CSA with CLA required more cells. So the power consumption and size requirement of the architecture is increases.

Rumi Rastogi, Sujata Pandey [3] proposed new architecture that is leakage power reduction in MTCOMS based high speed address to overcome the leakage power reduction along with reduces the power consumption. The COMS based static adders having leakage power problem. If is technology reduces this leakage power drastically increases, so low power technique introduced in this paper [3] that multi-threshold CMOS(MTCOMS) circuit design. This technique uses sleep transistor with high VT (Threshold Voltage). It is inserted between the logic circuit and supply (or) ground as header (or) footer. The circuit operates at high speed when the sleep transistor is ON in normal mode. The circuit is ideal mode when the sleep transistor is OFF and this case leakage power is minimized with slight delay and area increases. In this paper, the MTCMOS 130nm technology used and finally the authors are concluded that the average power and average leakage power are minimized compare to COMS technology but when the circuit is transistor form sleep mode to active mode large current flow through sleep transistor due to this large current cause the disturbance on real ground line and this is called the bounce noise and needs to be reduced. The power delay product (PDP) and delay are most constrains while designing the digital systems. The PDP is calculated by multiplying the worst case delay by average power consumption of the main circuit and the delay by are calculated from 50% of the input voltage level to 50% of output level.

Low power and full adder by exploring new XOR and XNOR gates [4] by Hamed Naseri and Somayeh Timarchi are proposed a novel XOR/XNOR gates for decreasing power delay product (PDP). The authors introduced the optimized width to length ratio of transistor is one approach to decrease PDP instead of decrease supply voltage. Based on the output voltage level the full adder is classified as full swing and non-full swing. The full swing full adder is complementary pass transistor logic (CPL) Transmission Gate (TG), 14T, 16T and hybrid pass logic with static CMOS output drive full adder (HPSC). The hybrid full adder mostly has two modules, XOR and XNOR gates and multiplexer. The XOR and XNOR gate consumers more power in designing of full adder so the minimization of power consumption in XOR – XNOR gate is more important than the minimization of power consumption of multiplexer. The proposed optimized method is transistor sizing method. In this transistor sizing method the transistor can be selected for optimum power delay product based on the transistor width and sizing methods. The transistor sizing tools are optimum and used in VLSI design for high performance of the architecture. The transistor sizing methods are two types. Method 1: The simulation time for optimizing the circuit is much reduced and this method is simple and fast but the drawbacks of this method is power dissipation and only delay reduces not PDP and accuracy also bad and another. Method 2: Proposed with accuracy and fast. The Particle Swarm Optimization (PSO) algorithm used for selecting the transistor sizing. For simulation 65nmCMOS process technology, 1.2v power supply voltage (VDD), maximum input frequency is 1GHZ. The proposed XOR – XNOR gates are reduces the delay and low power consumption by the absent of NOT gate. The output voltage is full swing, the smaller number of interconnection wires and layout is straight forward along with good output driving

capability. The proposed full adder having advantages optimum power consumption, delay reduced along with good output driving capability. To maintain good output driving capability additional buffer circuits are added in the design.

In [5] Ternary full adder using multi threshold voltage Graphene barristers by sunwoo Heo, sunmean kim et al., proposed a Ternary Full Adder to overcome the Multi Threshold Logic (MVL). This MVL reduces the complexity of interconnections along with the arithmetic operations. The MVL architecture using carbon nano tube FET, that can provide step wise V-I curve for various diameter (For the different threshold value) can be used in single device. But this analysis is ideal and theoretical. The MVL architecture using quantum dot gate FET provides three steps by controlling the charge state of quantum dot in gate dielectric but in this architecture the scalability of the device limited by charging and discharging. The ternary inverter uses the multi value logic by using Graphene Hetro-junction that shows light induced negative differential Transcondutance(NTR).The complementary ternary logic also uses the MVL by using graphene FET with both NPN and PNP channel profile. The both ternary and complementary ternary logic provide low thermal budget and high ON-OFF ratio and also V_{th} can controlled by schookly barrier potential height(SBH).but the performance is not good. So to improve the this ternary logic, proposed a new adder architecture of ternary logic using Multi Threshold Voltage Graphene Barristors(MTGB). This MTGB ternary is designed mainly by using the three different values of V_{th}. The ternary device switch with V_{th} =$|V_{th},0|$ for pull up/ pull down the network and the device with V_{th}= $|V_{DD}/2|$ is used for providing the stable noise immunity of half V_{DD} by using the negative feedback and V_{th}=$|V_{DD}$-$V_{th},0|$ is to generate the half V_{DD}. This ternary switch used in the proposed Ternary Full Adder and this proposed Ternary Full Adder reduces the power delay product, low thermal budget and high ON-OFF ratio and this proposed architecture not suitable for lower bit size because lower bit size require more area along with PDP.

3 REVERSIBLE LOGIC TECHNOLOGY (RLT).

The conventional IRLG are having unequal number of inputs and outputs. So it is no possible to recover the loosed energy or data. This loosed energy causes the heat dissipation and also reduces the performance of the unit. So to overcome that heat dissipation the RLG are used. This RLG improve the efficiency and speed. The RLG have equal number of inputs and equal number of inputs. The RLG are used in various applications like low power CMOS, optical communication, DNA computing, quantum computing and nano technology. The RLG having the following features, Fanout must be one, Garbage output equal number of inputs and equal number of outputs and hardware complexity. In [6] Maryam Rahmati, Monirech Housmand et al. Proposed a "novel design of a carry/barrow look-ahead adder/subtractor using reversible logic gates. And in this paper introduced the four different methods to design Carry Look-ahead Adder (CLA) based on reversible logic gates. In the first

method uses the 53 OR gates plus 37 AND gates plus 61 NOT gates this design having more quantum cost and garbage output. The second method designed with Fredkin, Feynman, R2 and TS4 gate, this design improves the quantum cost and reduces the Hardware complexity. The third method Feynman, Toffoli gate and Peres gates are used with improved quantum cost compare to first and second method. The fourth method designed with the less improvement. So the proposed paper main goal is CLA with less quantum cost, reduces the garage output and also reduces the delay. The proposed paper implemented two methods they are design 1: In this design Feynman and Peres gates are used to improve the quantum cost. The Peres gate has less quantum cost. The design 2: in this design uses the more gates to reduce the delay. However the proposed design1 have less power consumption and less Hardware complexity and the design2 has less delay.

In[7] J.W Bruce, M.A Thornton et. Proposed an Efficient adder circuit based on a conservative Reversible Logic Gates. The optimal logic gates perform the Irreversible logic functions based on the light pulses carry information or quantum (single photo carry information) levels with better efficiency. The all logic functions with optimal computing can't be realized. So to perform all logic functions with photons or atomic spin the qubits are used with quantum logic functions. The quantum logics are represented by unitary ortho normal matrices to represent the Reversible Logic Gates. The conservative Reversible Logic Gate has following principles a) balancing b) self invertible c) zero preserving d) controllable and conservative. The Fredkin Gate (FG) is one of the reversible logic gates and it is also called as controlled permutation gate. This FG can be used for the creating the inverse and signal duplication functions. The proposed architecture used the FG to implement the Ripple Carry Adder and Carry Skip Adder. The Ripple carry Adder with FG has reduced the signal Fan-out. The Carry Skip Adder with FG has reduced the delay along with carry propagation mechanism. The Carry Skip adder with FG can perform more complex functions. The carry Skip adder with FG can reduce the delay but Fan-out can be maintained so to reduce the Fan-out another gate can be added in the design

In general the testing of the circuit is required to ensure quality and reliability of the circuit. Novel approach for designing online testable Reversible Circuits by Md.selim Al Mamun at al [8]. The proposed approach for designing online Testable Reversible Circuits. This proposed approach uses the appropriate theorems and lemmas. A circuit is called online Testable if it is possible to test the circuit while performing the operations. This proposed approach mainly focus on the design online testable reversible circuit for detecting any single bit error in the circuit, for that the general idea used that convert each (n*n) reversible gate into (n+1)*(n+1) testable block which is also reversible. This additional $(n+1)^{th}$ output bit used to detect the error. This error bit of every testable block is carried to a checker circuit for producing the final error bit. The proposed approach has following steps. The first step is converting each Reversible Logic Gate in the circuit to Testable Reversible Gate (TRG). The TRG is also reversible. The second step is form the Testable Block (TB) by cascading the TRG. The third step is constructing the error checker circuit for the Testable

Block. This error checker block can be implemented by using the modified Fredkin Gate. All these steps use the appropriate theorems and lemmas to clarify the proposed design. This proposed architecture works with any Reversible Logic circuit. The testable reversible circuits have higher logic levels than the standard logic levels. The proposed design is efficient in terms of number of gates, delay and garbage output.

The general method of constructing the Reversible Full Adder is proposed by Lihui Ni, Zhijin Guan at al [9]. The proposed approach used to verify the design of Reversible Full Adder with two Reversible Gates and two garbage output. This proposed design improves the gate count, garbage count and reduce the cost of the network. The general 3 bit Full adder has sum=A⊕B⊕C---- (1) and carry =AB⊕(A⊕B)C_{in}---- (2). This general 3 bit full adder using three inputs and two outputs. The input vector can construct the output vector but it is not possible in this general full adder because number of inputs is not equal to the number of outputs. So to make the reversible circuit adds an additional two garbage outputs at the output for making the combinations unique. The proposed method can be created by using two 3 inputs/outputs Reversible gate with 2 garbage outputs. The proposed method has following steps. In step one assume M=A⊕B and substitute in equation one, then equation one becomes S=M⊕C_{in}. In next step assume N=AB and substitute in equation two, then equation two becomes C_{out}=N⊕MC_{in} The final step is to implement the RFA make one constant signal among the three input signals. If C=0, the output equation should be M=A⊕B, N=AB and with one garbage output G. The proposed approach is optimal in regard to garbage count.

Kamalakannan.V, Shilpkala.V and Ravi H. N proposed a novel adder/subtractor circuits based on Reversible Gates [10]. The analysis of proposed architecture is verified in terms of number of reversible gates, number of garbage inputs/outputs and quantum cost. Toffoli gate, Peres gate, Fredkin gate and TR gate are some of the examples of reversible logic gates. Any reversible gate can be realized by using the 1*1 NOT gate and 2*2 reversible gate such as V &V^+(where V is square root of NOT, and V^+ is it's hermitian) and this V&V^+ have the following properties V*V=NOT, V*V^+=V^+*V=I and V^+*V^+=NOT. The quantum cost of the reversible logic gates can be calculated by counting V, $V^+$and CNOT. The main objective of proposed approach is implementing the Reversible Full Adder/Subtractor in single unit. This paper proposed 3 different types of Full Adder/Subtractor implementations. The first proposed design is FULL-ADDER-SUBTRACTION-MUX with Peres gates for addition operation.TR gates for the subtraction operation and FG for Multiplexing carry& borrow line into single line output. This proposed architecture used total 8 RG. Another proposed method is FULL-ADDER-SUBTRACTOR-TR gate with TR gates for addition and subtraction operations, The Feynman gates for input signal buffering. In this method the quantum cost is improved compare to first method. The last proposed method is FULL-ADDER-SUBTRACTOR-HYBRID with Feynman gates for addition and subtraction operations. The Fredkin and TR gates for carry realization and borrow realization. This is an optimized method because the optimum values of quantum cost, garbage inputs/outputs are obtained. These proposed methods

are useful in low power applications where both adder/subtraction are required. The proposed design reduces the delay and power compare to conventional logic gates.

4 CONCLUSION

In this paper various designing methods are discussed for digital system applications using both irreversible and reversible techniques. From literature the irreversible logic gates are simple to design but various problems are occurred like voltage swing, more area, power consumption and noise occurring problem, To overcome these drawbacks the reversible logic technology used. The reversible have many advantages like equal number of inputs and outputs, minimize the garbage output and minimizes the power consumption. It also provide that the reversible logic gates improves the energy efficiency and velocity of nano circuits

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