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Real-Time Magnetic Measurement Monitoring under cRIO-LabVIEW Based Platform

Pasquale Arpaia, Vincenzo Di Capua, Marco Roda and Marco Buzio

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1st Pasquale Arpaia
DIETI-IMPALAB
University of Naples Federico II
Napoli, Italy
pasquale.arpaia@unina.it

2nd Vincenzo Di Capua
TE-MSC-MM
CERN, European Organization for Nuclear Research
Geneva, Switzerland
vincenzo.di.capua@cern.ch

3th Marco Roda
TE-MSC-MM
CERN, European Organization for Nuclear Research
Geneva, Switzerland
marco.roda@cern.ch

3th Marco Buzio
TE-MSC-MM
CERN, European Organization for Nuclear Research
Geneva, Switzerland
marco.buzio@cern.ch

***Abstract*—At CERN, six synchrotrons use a so-called B-train system to measure the field of the bending magnets and to distribute it in real-time to various users, including the RF subsystem, via White Rabbit (WR). This paper proposes an improvement for the read-out and debugging of the distributed field values. Currently, the magnetic field produced by a given current applied to a certain reference magnet is monitored by decoding the WR frame payload and plotting the output signals with a Python GUI-based application running on a workstation connected with the receiving WR switch. This set-up is limited since there is no mechanism to access it remotely; more importantly, the Python application does not support real-time time-stamped debugging and alarms, which are crucial features to detect possible faults and link the signals to the operational status of the accelerators. A new monitoring system was developed in order to provide simple remote access to the B-train signals and to add the missing time-stamp feature. This paper presents the developed hardware and software, together with the results of the first validation tests.**

***Index Terms*—Magnetic Measurements, Real-Time, B-train, White Rabbit, cRIO platform, LabVIEW, FPGA.**

I. Introduction

Precise and real-time knowledge of the bending magnetic field is essential for the correct operation of a synchrotron-type particle accelerator. For the superconducting magnets of the Large Hadron Collider (LHC) at CERN, mathematical models are sufficient to predict the actual magnetic field in the machine. In resistive magnets [1] [2] the field produced by a given current is not always predictable to the required accuracy (e-4) with a mathematical model due to several effects: iron hysteresis; eddy currents; temperature drifts; material aging and hysteresis. Therefore, at CERN all the other six synchrotrons including the LHC injector chain rely on the instantaneous average bending field measurement for longitudinal and transversal beam control, beam diagnostics, radio frequency cavity control, power supply control and qualitative feedback for operators. The measurement is typically carried out in a reference magnet, powered in series with the ring, by means of measurement systems called B-trains.

The B-train system consists of a real-time magnetic field measurement where a flux-coil is placed in the magnet aperture generating an induced voltage. This voltage is proportional to the field time derivative and acquired using an analog-to-digital converter (ADC). The digital output is then integrated producing $B(t)$. As integration constant, an additional sensor is used as a field marker. This triggers a TTL signal whenever a certain programmed B value is reached. The computed calculation for the magnetic field $B(t)$ can be seen in Equation 1.

$$B(t) = B_0 + \frac{1}{A_c}\int_{t_0}^{t} V_c \, dt \tag{1}$$

where B_0 refers to the magnetic field at t_0, A_c to the surface area of the coil and V_c to the induced coil voltage.

Currently, all six B-train system in operation are being revamped in the frame of a long-term complex-wide consolidation project. In particular, WR is being implemented as a modern replacement for the legacy digital transmission (dating from the early 1960's), which was based on two 24 V pulse lines transmitting the field by increments of +- 0.1 Gauss.

The new distribution allows to overcome a number of limitations such as the bandwidth (250 kHz), the reach limited to a few hundred meters, and the relatively low reliability due to the need of signal repeaters. The new B-trains will need to update field measurements as fast as one MHz to keep up with upcoming, fast-cycled magnets (for the PS Booster upgrade), and to distribute them as far as several kilometers (for the new SPS beam dump system).

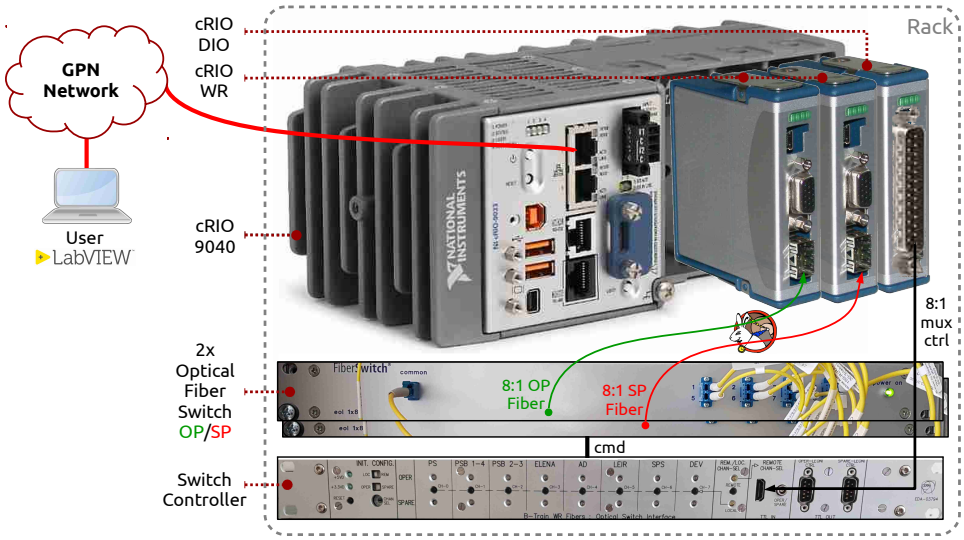

Fig. 1. B-train monitoring proposed architecture.

Monitoring the WR payloads at full speed and for extended periods of time is an essential part of both, the commissioning and operation phases. Initially, system debugging requires that the measurements distributed via WR be compared systematically to old measurements and to the signals as received by the numerous end users. Noise and glitches in the field measurement can affect destructively the beams and require full bandwidth to be evaluated correctly. In operation, continuous comparison of twin parallel acquisition chains to each other and to expectations (simplified mathematical models) will be needed to diagnose instrumentation errors such as integrator drift, identify fault conditions in order to raise the appropriate alarms, and to evaluate measurement uncertainty estimates.

So far, a Python-based acquisition system has been used to intercept the WR stream and save it to file. This implements a Direct Memory Access (DMA) to retrieve upcoming White-Rabbit (WR) data previously stored on a Double Data Rate (DDR) memory. There are some drawbacks on this solution, such as: not easy customization; not easy installation procedure; impossibility to check simultaneously multiple measurement chains; no remote access and impossibility to select remotely the system to be monitored and debugged.

In this paper, a novel real-time cRIO-LabVIEW based system for B-train status monitoring and debugging is presented. Section II describes the architecture implemented in the prototype. The block diagram and its modules are presented in section III; data flow and design choices are described in detail. The hardware description language (HDL), software development and the operation of the graphical user interface (GUI) are presented in section IV. Finally, in section V some conclusions and future work are drawn.

II. Proposed Architecture

The strong requirements in terms of flexibility and remote access, led the development to use the CompactRIO (cRIO) platform from National Instruments (NI). The optical fibers, chosen physical link to broadcast the measurement signals, arrive to two optical fiber switches from the operational (OP) and spare (SP) chains. To decode the WR B-train data, a cRIO White Rabbit module (CRIO-WR) [3] was used. CRIO-WR is a standalone WR node implementation on a PCB with a form factor for NI cRIO crates. The board is originally derived from and keeps maximum firmware compatibly with the established boards SPEC [4] and CUTE-WR [5]. To control the optical fiber switch, a DIO module NI-9401 connected to a Switch Controller was used.

To host and control the CRIO-WR and the DIO modules, a cRIO crate controller NI-cRIO-9040 is used. The processor runs a real-time software target used to access the device and therefore the B-train data from any PC on the same network with an Ethernet connection. A simple overview of the proposed architecture is depicted in Fig. 1

III. Block Diagram

A. cRIO-9040 Embedded Controller

The cRIO-9040 is a four slot high performance embedded controller from NI. Within the controller there is a Xilinx FPGA Kintex-7 series and a dual core Intel Atom running NI Linux RealTime at 1.3 GHz. It manages the connection between the controller and a host PC over Ethernet. This device communicates with the cRIO modules collecting the data coming from the CRIO-WR node and addressing the optical fiber switch through the cRIO-DIO.

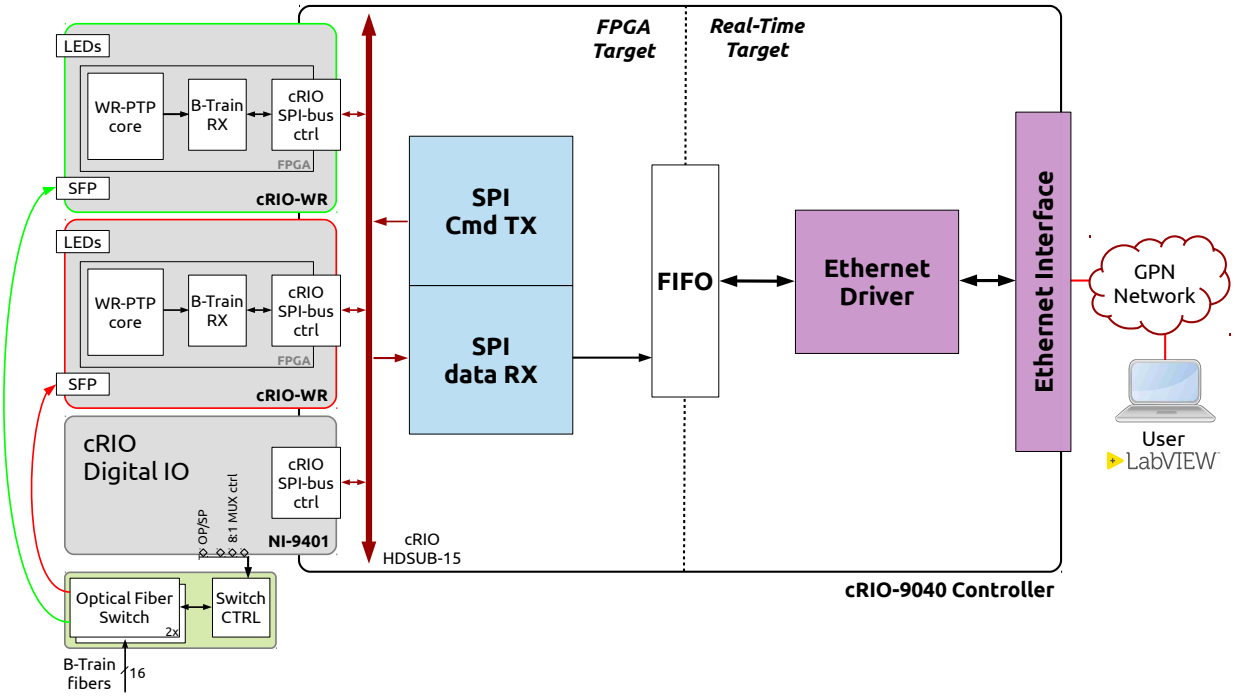

Fig. 2. Block diagram of the B-train monitoring system.

B. cRIO White Rabbit Module

CRIO-WR [3] is a custom board with native WR support based on a XC6SLX45T Spartan-6 FPGA. The FPGA gateware includes the WR Precision-Time-Protocol (PTP) Core [6] [7], the WR streamers [8] [9], the needed logic to extract and decode the BTrain over WR and the cRIO SPI interface. In addition, some glue logic is used to allow a good interface between the FPGA modules.

C. NI-9401 DIO Module

The NI-9401 [10] is a configurable digital I/O module working between 0 V and 5 V TTL. In this application it controls the optical fiber switch, selecting the machine (measurement chain) to be debugged and monitored. The switch is a multiplexer, three digital lines are necessary to select one of the 8 machines remotely and a fourth line to select between OP and SP.

D. Data Flow

Optical fibers coming from the various B-Train and connected to the optical fiber switch, as presented in Fig. 2, are plugged into the CRIO-WR module. The WR PTP Core and the streamers extract the Ethernet payload sent via WR and pass it to the BTrain receiver module decoding the raw signals forming the B-frame (Fig. 3). In the current implementation a new valid frame arrives every 4 μs (250 kHz); depending on the command byte from the controller, certain frame slots are transfered to the FPGA target.

In this proof-of-concept, header, B, Bdot and oldB are sent. This module takes care of sending the data to the controller's FPGA via cRIO interface.

The structured data arrive to the FPGA target, in which, a comparison is performed to avoid the process of the same frame twice. The data pass then through a FIFO to cross the two clock domains present inside the FPGA target, 40 MHz and 5 MHz. The header status information, B, Bdot and oldB raw values are pulled from the structure payload and filled into a FIFO, one for each slot. Data is then retrieved by the host application through the Ethernet interface. Thanks to the real-time target, received and decoded data are sent to the network and to the host PC on the same subnetwork of the chassis. On the host side, data are collected and elaborated to be plotted and logged into files.

IV. VHDL and Software Development

A. cRIO-WR FPGA Gateware

The FPGA gateware on the CRIO-WR module was developed starting from an example project available on the CERN Open Hardware Repository [3]. The existing demo project contains only the WR-PTP core and it basically sends a time-stamp of few bytes. To reach the desired goals, some blocks were added: Streamers to extract the Ethernet payload out of the WR PTP core; BTrain Transceiver (B-Train RX) to decode the user-specific B and I Frame [11]; and cRIO SPI-bus controller to send/receive data to/from the cRIO embedded controller. For the time being, only B-frames are taken into account. They are identified through the header and latched out when a new valid frame arrives. The cRIO SPI-bus controller block is then transmitting the data into the cRIO controller.

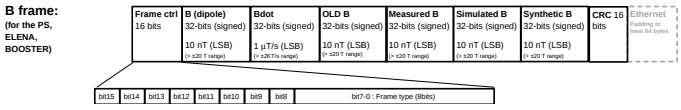

Fig. 3. White Rabbit B-frame.

B. FPGA Kintex-7 70 T

The cRIO controller's embedded FPGA collects the data from the CRIO-WR modules and provides the decoded signals to the host user application. On the FPGA there are two different clock domains, 40 MHz for the SPI interface with the CRIO-WR modules and 5 MHz for the host application and DIO module interface. The data, at the controller's FPGA target, is then connected to the cross clock domain FIFO (2k samples of 14 bytes), in which its output is split into 5 different signals, the WR B-frame slots. To have all slots synchronized and aligned for plotting on the host application, five FIFOs are needed.

The used FIFOs have a capacity of 2024 samples of 32 bits on the target side and a capacity of 250k samples of 32 bits on the host side. This values have been calculated in order to avoid timeouts caused by overflow.

The DIO module is also controlled by this FPGA. It drives the switch controller and multiplexes the 16 optical fiber switch inputs to its 2 outputs, OP and SP chains. The fibers are then connected to the CRIO-WR and processed resulting in 16 different monitored systems with only two fiber SFP port inputs.

C. LabVIEW Host Application

On the host side, a dedicated LabVIEW user application was developed. At each start of its VI, the depth of the FIFOs is initialized as described above (5x 250k sample FIFOs of 32 bits each).

A main while loop reads-out and extract the data from the 32 bits five slots. A scaling factor is then applied and samples are decimated. The decimation is performed to shrink the decoded samples for plotting purposes.

As shown in Fig. 4, there are two graphs, one for B, old B and C0 and a separate one for Bdot. Each waveform on the graphs can be enabled or disabled depending on the analysis to be performed.

In a second loop, based on events, the multiplexer is controlled to select which measurement chain to be plotted. It is also possible to log the signal waveforms into .tdms and/or .txt files for further post processing with other tools, assuring a correct time synchronization due to the White Rabbit protocol implementation.

V. Conclusion

We presented a new real-time WR monitoring and debugging system, based on a Compact RIO platform and on a cRIO-WR module, to improve flexibility and remote access to the signals of the new B-Trains at CERN. A proof of concept was successfully obtained under a platform never used

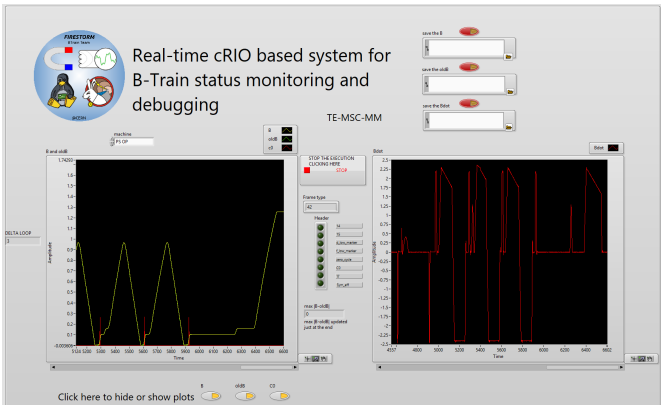

Fig. 4. Front panel of the LabVIEW host user application.

previously in this context, demonstrating that the requirements in term of both performance and operational flexibility can be met.

This work showcases the power and possibilities offered by WR, as a new and flourishing standard in the general context of distributed acquisition and control system, especially when accurate timing and synchronization are important.

This monitoring device will cover a key role in the final implementation of the new B-train system at CERN, as it will allow real-time data logging, monitoring and visualization of multiple data streams to an unprecedented level of accuracy and resolution. In the immediate future, our work will be focused on sending and decoding the entire field and current frame payloads, and develop a user friendly mechanism to log the data into files or even a database accessible from a web application.

Acknowledgment

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